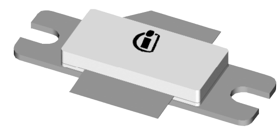
Thermally-Enhanced High Power RF LDMOS FETs 130 W, 869 – 960 MHz

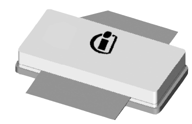
Description

The PTF081301E and PTF081301F are 130-watt, internally-matched *GOLDMOS* FETs intended for EDGE and CDMA applications in the 869 to 960 MHz bands. Thermally-enhanced packaging provides the coolest operation available. Full gold metallization ensures excellent device lifetime and reliability.

PTF081301E
Package 30248

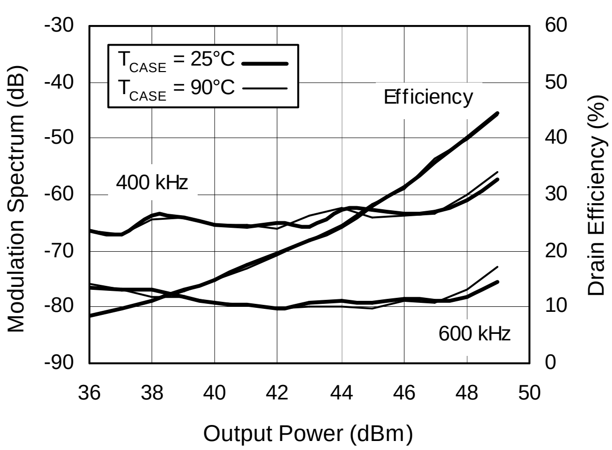


PTF081301F
Package 31248



EDGE Modulation Spectrum Performance

V_{DD} = 28 V, I_{DQ} = 950 mA, f = 959.8 MHz



Features

- Thermally-enhanced packages
- Broadband internal matching
- Typical EDGE performance
  - Average output power = 65 W
  - Gain = 18 dB
  - Efficiency = 40%
- Typical CW performance
  - Output power at P–1dB = 150 W
  - Gain = 17 dB
  - Efficiency = 55%
- Integrated ESD protection: Human Body Model, Class 1 (minimum)
- Excellent thermal stability
- Low HCI drift
- Capable of handling 10:1 VSWR @ 28 V, 130 W (CW) output power

RF Characteristics

EDGE Measurements (not subject to production test—verified by design/characterization in Infineon test fixture)

V_{DD} = 28 V, I_{DQ} = 950 mA, P_{OUT} = 65 W, f = 959.8 MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Error Vector Magnitude	EVM (RMS)	—	2.5	—	%
Modulation Spectrum @ 400 kHz	ACPR	—	–62	—	dBc
Modulation Spectrum @ 600 kHz	ACPR	—	–74	—	dBc
Gain	G_{ps}	—	18	—	dB
Drain Efficiency	η_D	—	40	—	%

All published data at T_{CASE} = 25°C unless otherwise indicated

ESD: Electrostatic discharge sensitive device—observe handling precautions!

RF Characteristics (cont.)

Two-Tone Measurements (tested in Infineon test fixture)

V_{DD} = 28 V, I_{DQ} = 950 mA, P_{OUT} = 130 W PEP, f = 960 MHz, tone spacing = 1 MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Gain	G_{ps}	17	18	—	dB
Drain Efficiency	η_D	40	42	—	%
Intermodulation Distortion	IMD	—	–32	–29	dBc

DC Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_{DS} = 10 µA	$V_{(BR)DSS}$	65	—	—	V
Drain Leakage Current	V_{DS} = 28 V, V_{GS} = 0 V	I_{DSS}	—	—	1.0	µA
On-State Resistance	V_{GS} = 10 V, I_{DS} = 1 A	$R_{DS(on)}$	—	0.1	—	Ω
Operating Gate Voltage	V_{DS} = 28 V, I_{DQ} = 950 mA	V_{GS}	2.5	2.9	4.0	V
Gate Leakage Current	V_{GS} = 10 V, V_{DS} = 0 V	I_{GSS}	—	—	1.0	µA

Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	V
Gate-Source Voltage	V_{GS}	–0.5 to +12	V
Junction Temperature	T_J	200	°C
Total Device Dissipation	P_D	473	W
Above 25°C derate by		2.70	W/°C
Storage Temperature Range	T_{STG}	–40 to +150	°C
Thermal Resistance (T_{CASE} = 70°C)	$R_{\theta JC}$	0.37	°C/W

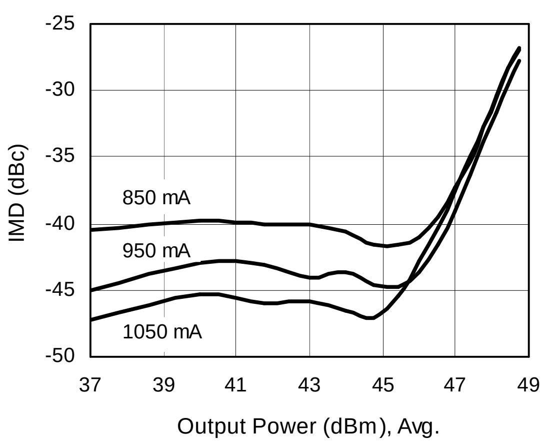
Ordering Information

Type	Package Outline	Package Description	Marking
PTF081301E	30248	Thermally-enhanced slotted flange, single-ended	PTF081301E
PTF081301F	31248	Thermally-enhanced earless flange, single-ended	PTF081301F

Typical Performance (measurements taken in production test fixture)

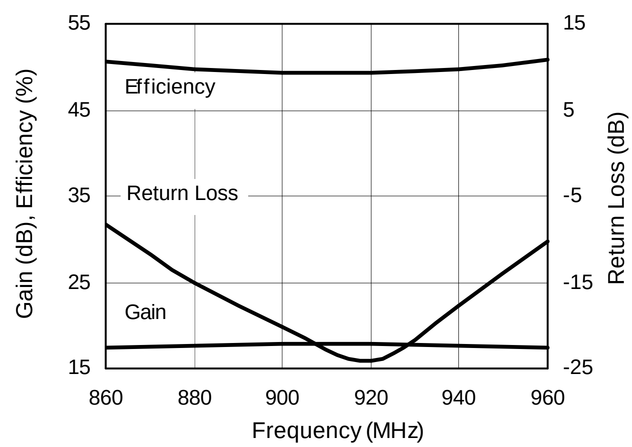
IM3 vs. Output Power at Selected Biases

V_{DD} = 28 V, f_1 = 959, f_2 = 960 MHz, series show I_{DQ}



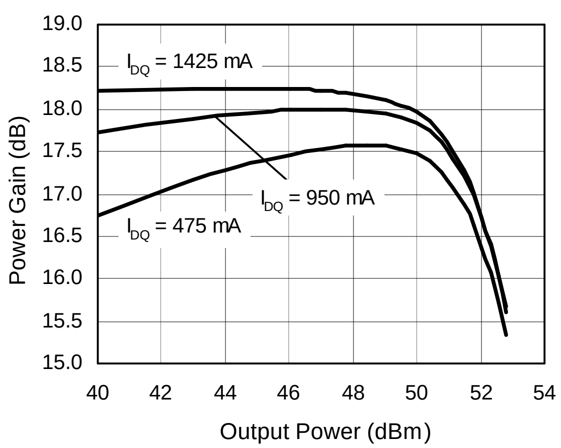
Broadband Performance

V_{DD} = 28 V, I_{DQ} = 950 mA, P_{OUT} = 51.14 dBm



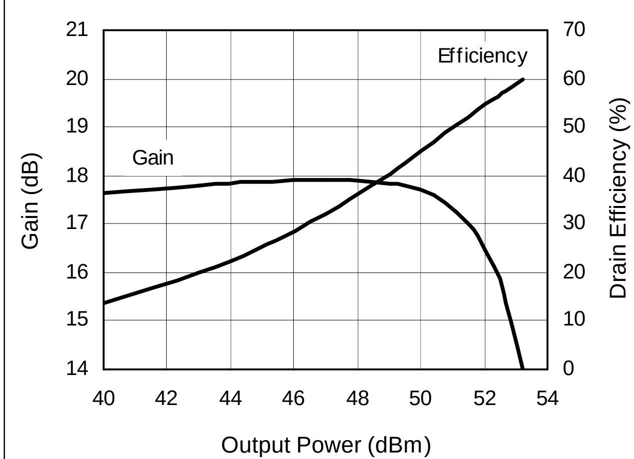
Power Sweep

V_{DD} = 28 V, f = 960 MHz

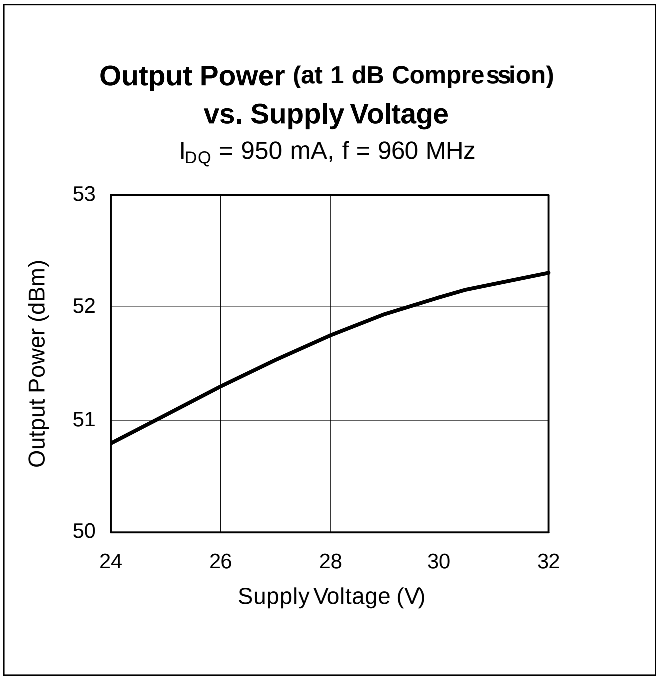


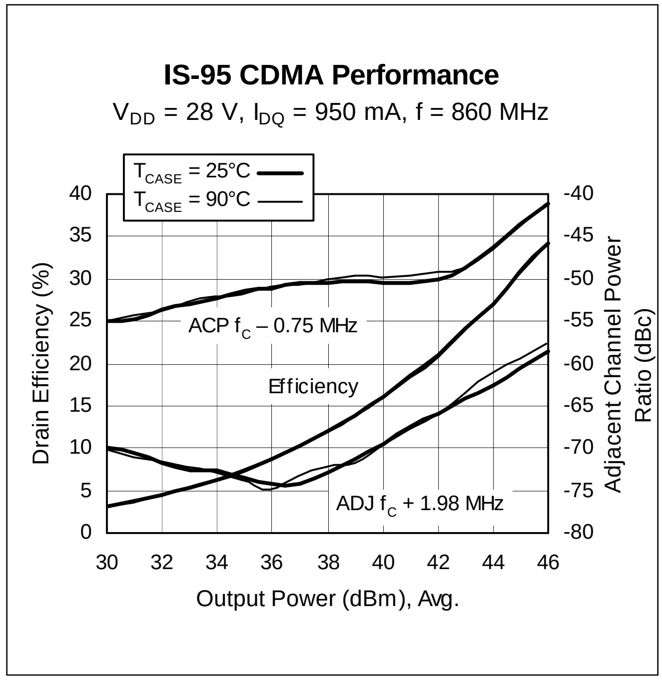
Gain & Efficiency vs. Output Power

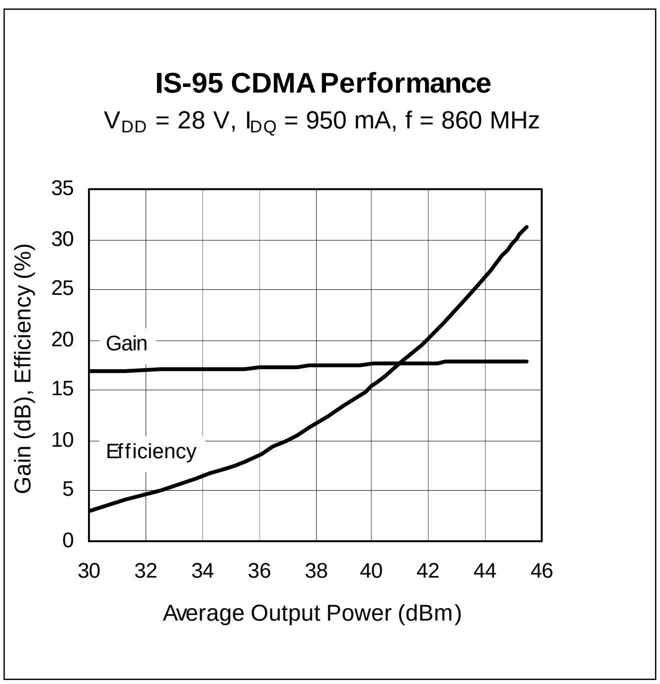
V_{DD} = 28 V, I_{DQ} = 950 mA, f = 960 MHz

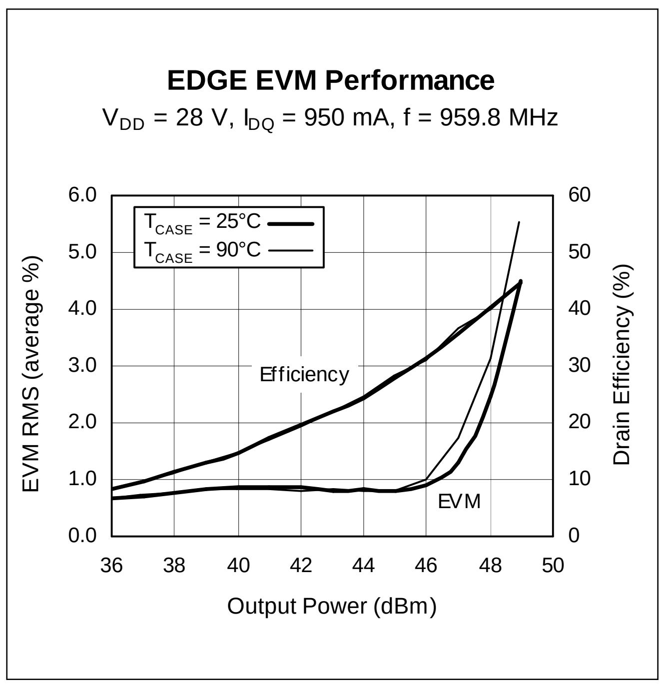


Typical Performance (cont.)

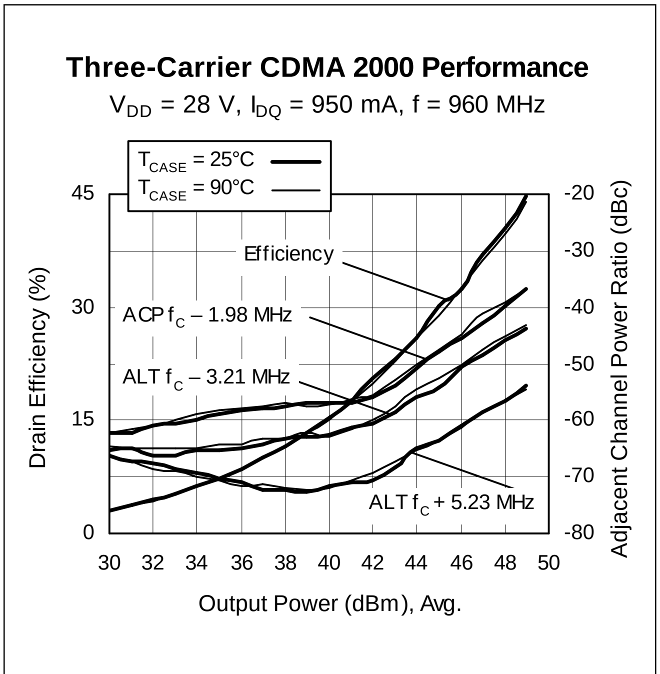


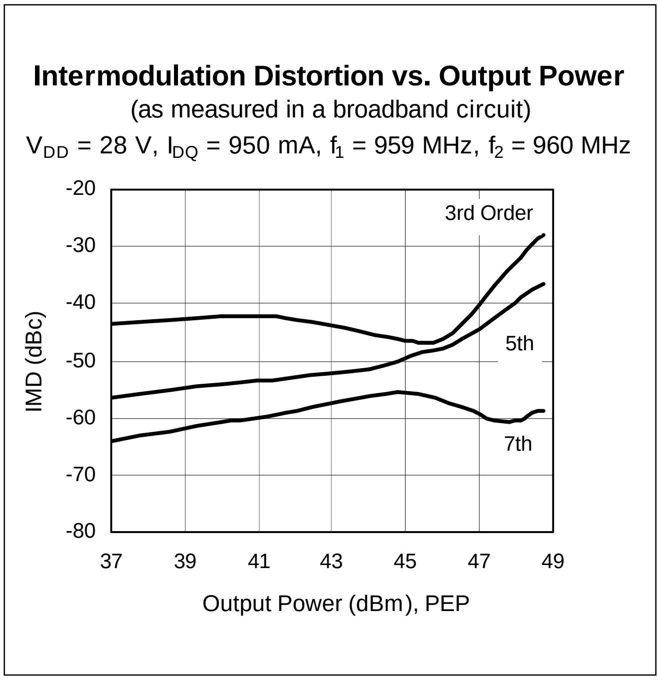


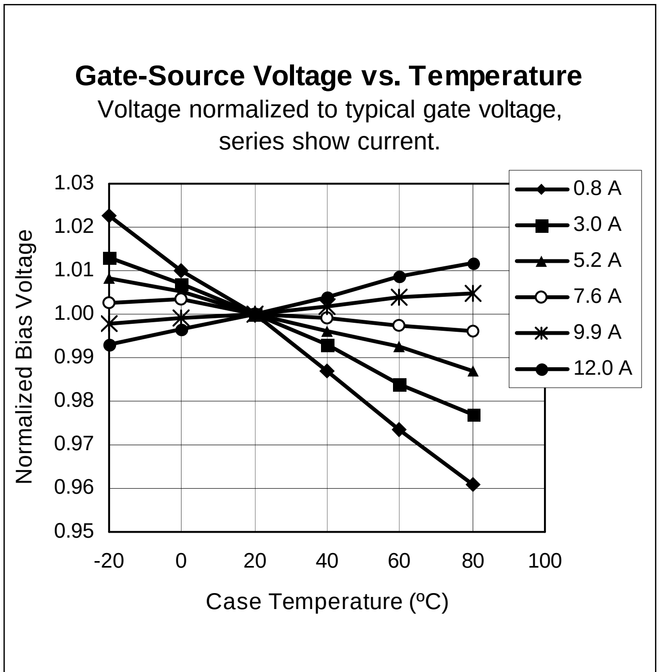




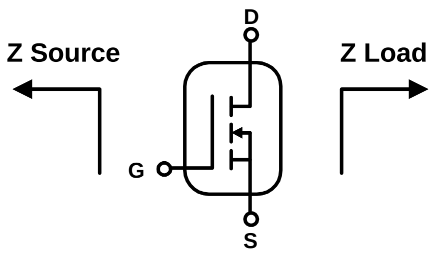
Typical Performance (cont.)

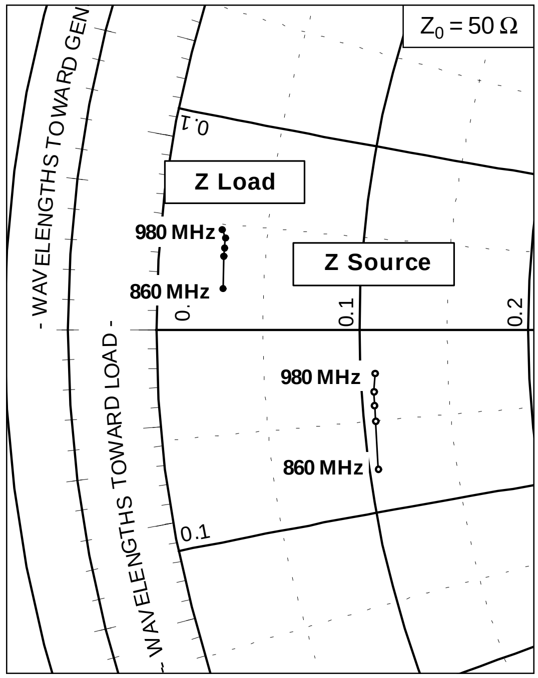






Broadband Circuit Impedance

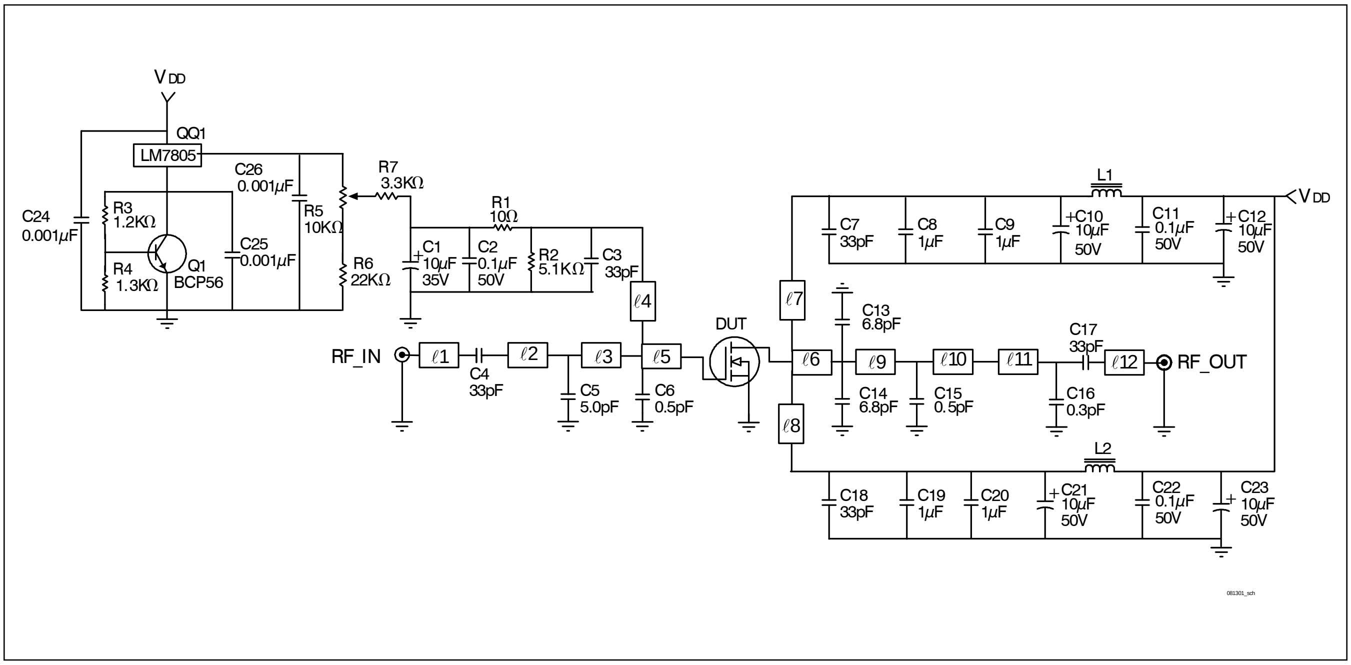




Frequency	Z Source Ω		Z Load Ω	
MHz	R	jX	R	jX
860	5.35	–3.80	1.59	0.99
920	5.41	–2.54	1.56	1.74
940	5.43	–2.16	1.56	1.91
960	5.42	–1.70	1.56	2.15
980	5.48	–1.24	1.50	2.34

See next page for Reference Circuit

Reference Circuit



Reference Circuit Schematic for 960 MHz

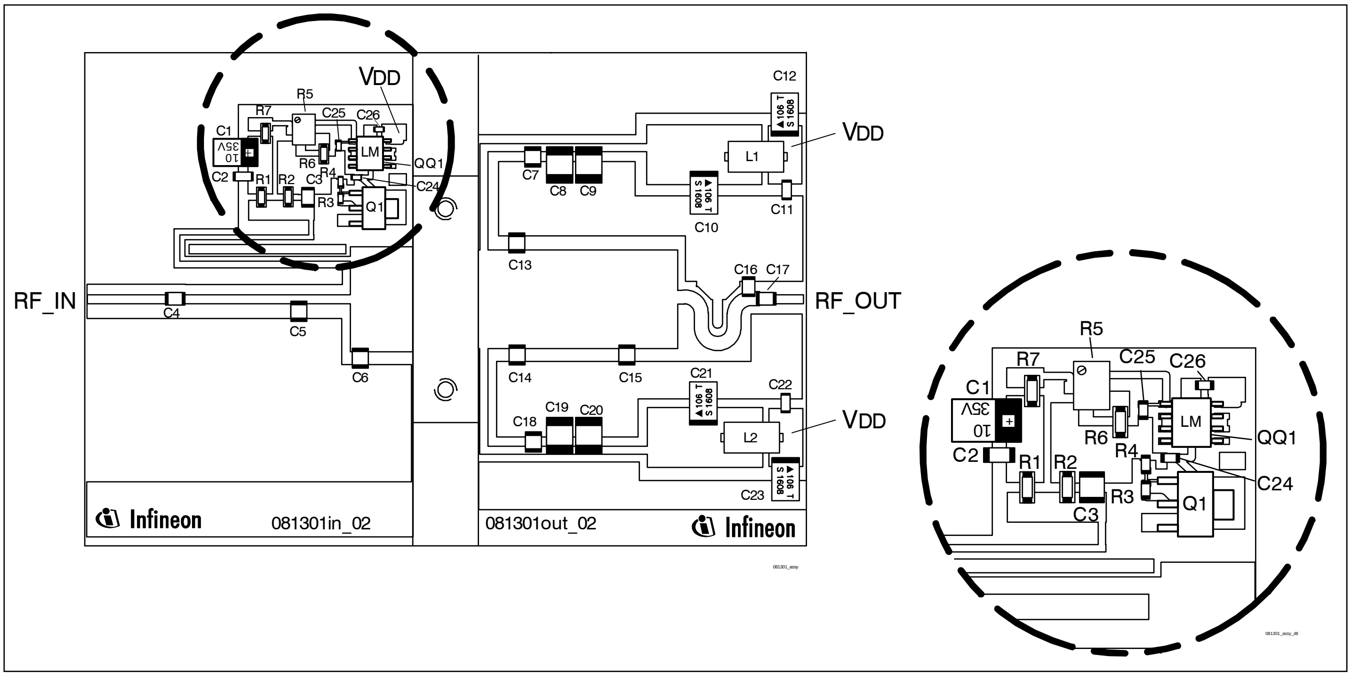
Circuit Assembly Information

DUT	PTF081301E or PTF081301F	LDMOS Transistor	
PCB	0.76 mm [.030"] thick, ε_r = 4.5	2 oz. copper	Rogers TMM4

Microstrip	Electrical Characteristics at 960 MHz[1]	Dimensions: L x W (mm)	Dimensions: L x W (in.)
ℓ1	0.075 λ, 50.0 Ω	12.70 x 1.35	0.500 x 0.053
ℓ2	0.101 λ, 50.0 Ω	17.27 x 1.35	0.680 x 0.053
ℓ3	0.055 λ, 50.0 Ω	9.40 x 1.35	0.370 x 0.053
ℓ4	0.289 λ, 74.0 Ω	50.80 x 0.64	2.000 x 0.025
ℓ5	0.061 λ, 7.5 Ω	9.27 x 16.26	0.365 x 0.640
ℓ6	0.036 λ, 7.9 Ω	5.46 x 15.24	0.215 x 0.600
ℓ7, ℓ8	0.132 λ, 50.0 Ω	22.61 x 1.27	0.890 x 0.050
ℓ9	0.114 λ, 7.9 Ω	17.40 x 15.24	0.685 x 0.600
ℓ10	0.047 λ, 7.9 Ω	7.24 x 15.24	0.285 x 0.600
ℓ11	0.134 λ, 38.0 Ω	22.35 x 2.16	0.880 x 0.085
ℓ12	0.029 λ, 50.0 Ω	4.95 x 1.37	0.195 x 0.054

[1]*Electrical characteristics rounded*

Reference Circuit (cont.)



Reference Circuit (not to scale)*

Component	Description	Suggested Manufacturer	P/N or Comment
C1	Tantalum capacitor, TE Series, 10 µF, 35 V	Digi-Key	PC56106-ND, SMD
C2, C11, C22	Capacitor, 0.1 µF, 50 V, 1206	Digi-Key	PCC104BCT-ND
C3, C4, C7, C17, C18	Capacitor, 33 pF	ATC	100B 330
C5	Capacitor, 5.0 pF	ATC	100B 5R0
C6, C15	Capacitor, 0.5 pF	ATC	100B 0R5
C8, C9, C19, C20	Capacitor, 1 µF, 50 V	Digi-Key	19528-ND
C10, C12, C21, C23	Tantalum cap, 10 µF, 50 V, TPS Series, SMD	Garrett Electronics	TPSE106K050R0400
C13, C14	Capacitor, 6.8 pF	ATC	100B 6R8
C16	Capacitor, 0.3 pF	ATC	100B 0R3
C24, C25, C26	Capacitor, 0.001 µF, 50 V, 0603	Digi-Key	PCC1772CT-ND
L1, L2	Ferrite, 6 mm	Ferroxcube	53/3/4.6-452
Q1	Transistor	Infineon	BCP56
QQ1	Voltage regulator	National Semiconductor	LM7805
R1	Resistor, 10 ohms, 1/4 W, 1206	Digi-Key	P10ECT-ND
R2	Resistor, 5.1 k-ohms, 1/4 W, 1206	Digi-Key	5.1KECT-ND
R3	Resistor, 1.2 k-ohms, 1/10 W, 0603	Digi-Key	P1.2KGCT-ND
R4	Resistor, 1.3 k-ohms, 1/10 W, 0603	Digi-Key	P1.3KGCT-ND
R5	Potentiometer, 10 k-ohms, 0.25 W	Digi-Key	3224W-103ETR-ND
R6	Resistor, 22 k-ohms, 1/10 W, 0603	Digi-Key	P22KGCT-ND
R7	Resistor, 3.3 k-ohms, 1/4 W, 1206	Digi-Key	P3.3KECT-ND

**Gerber files for this circuit are available on request.*

Package Outline Specifications

Package 30248

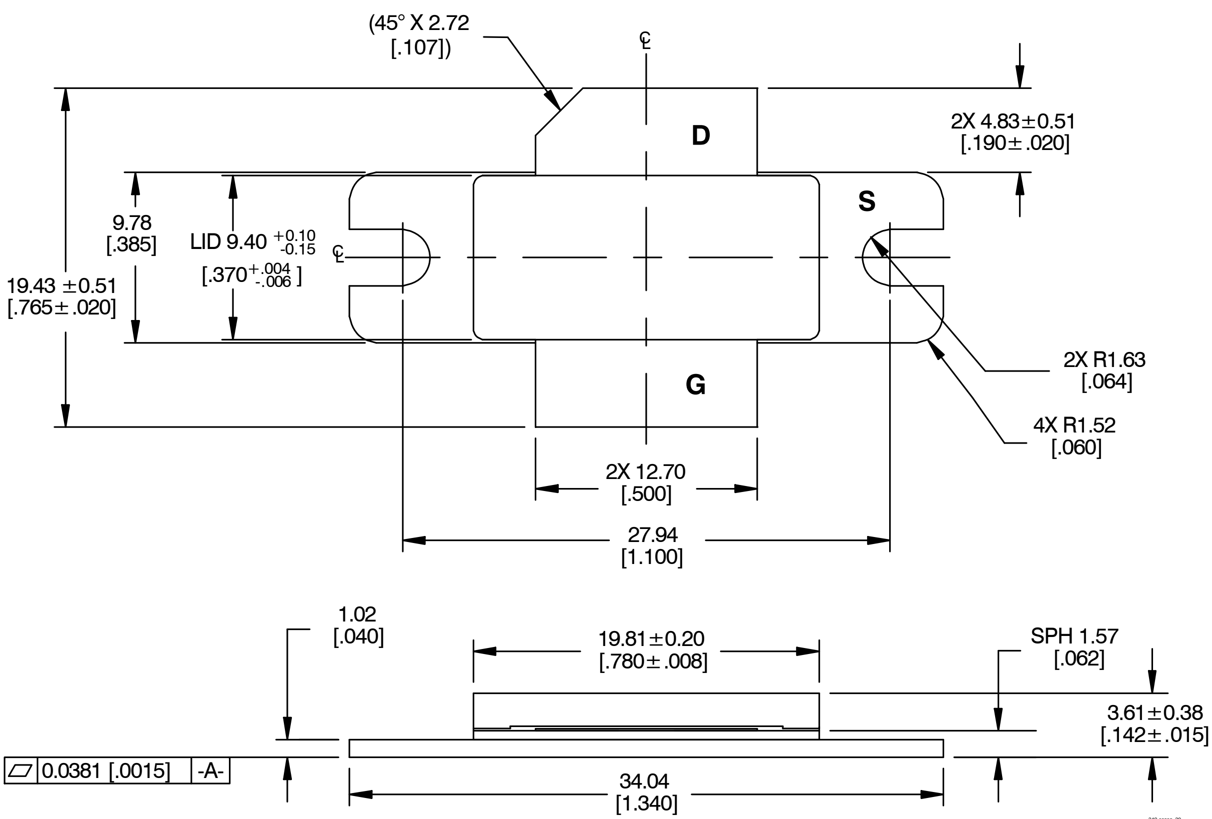


Diagram Notes:

1. Lead thickness: 0.10 +0.051/–0.025 [.004 +.002/–.001].
2. All tolerances ± 0.127 [.005] unless specified otherwise.
3. Pins: D = drain, S = source, G = gate.
4. Interpret dimensions and tolerances per ASME Y14.5M-1994.
5. Primary dimensions are mm. Alternate dimensions are inches.
6. Gold plating thickness:
   S - flange: 2.54 micron (min) [100 microinch (min)]
   D, G - leads: 1.14 micron ± 0.38 micron [45 microinch ± 15 microinch]

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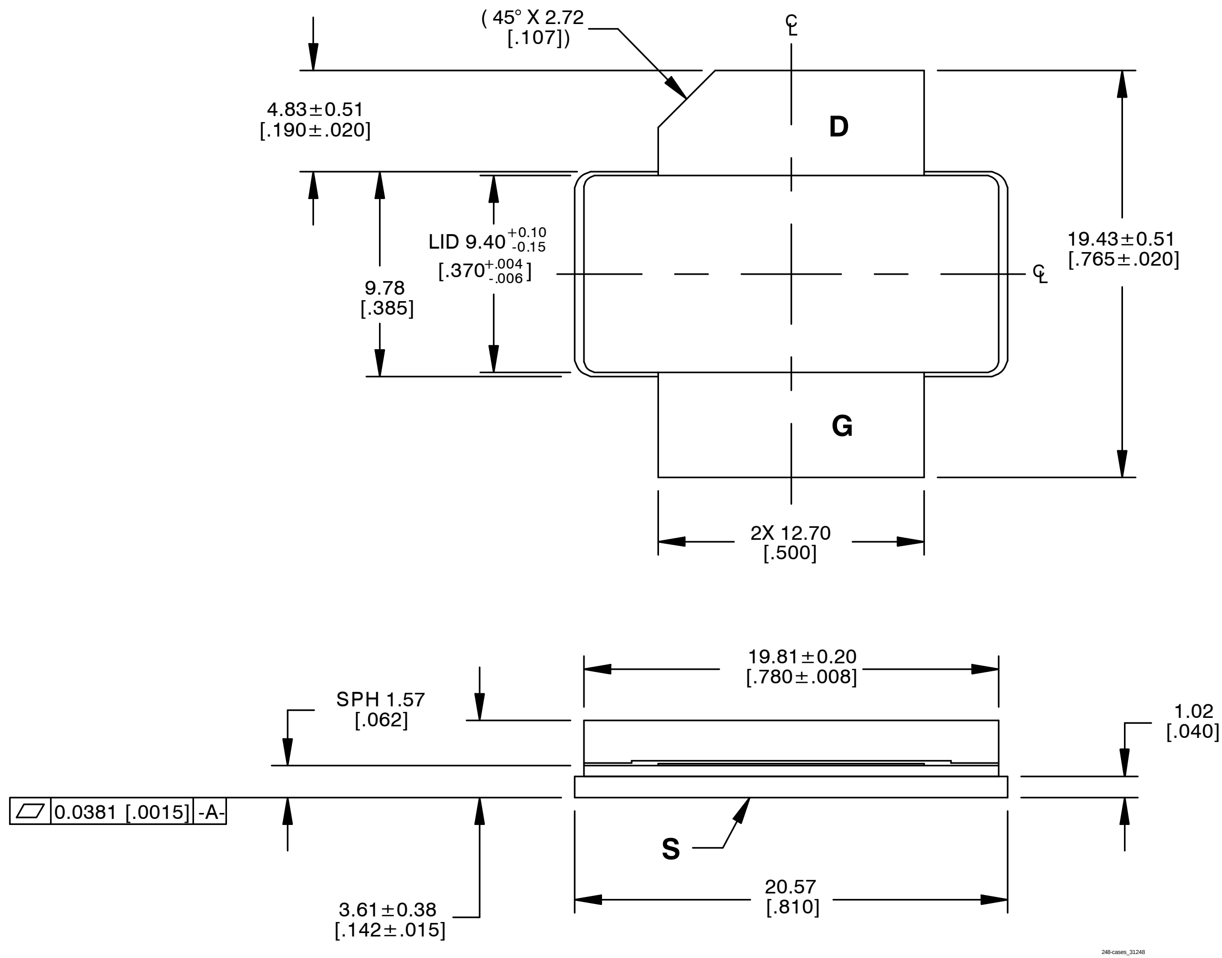
Package Outline Specifications (cont.)

Package 31248



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Revision History:	**2005-05-02**	Data Sheet
Previous Version:	2004-08-27, Data Sheet	

Page	Subjects (major changes since last revision)
1, 2	PTF081301F released
7, 8	Circuit descriptions
9, 10	Add and revise case outlines

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